High-Performance Gate-all-around Junctionless Vertical-Channel Transistors with the Ultra-low Sub-threshold Swing for Next-generation 4F^2 DRAM

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***Abstract*—** In this paper, we have successfully fabricated the junction-less GAA VCT combined with a hexagonal capacitor to realize a compact 4F^2 DRAM architecture. It shows the breakthroughs of I_{on}/I_{off}>10^9 and *SS*=62.5 mV/dec. We also elaborated on various key process issues and device parameters and how they impact on performance.

Keywords: Vertical channel transistor, Junction-less transistor, Gate-all-around, 4F^2 DRAM, Hexagonal capacitor.

I. INTRODUCTION

As one of the best-selling memory chips, DRAM has merits in cell size, storage capacity, operation speed, cost as well as a relatively simple structure and manufacturing process rather than other memories. Advancements from the continuous enhancement of lithography capability with 1T1C structure (**Fig. 1**), it is the well-known method for DRAM to achieve a higher density with lower cost by shrinking a minimum feature size. Compared with 6F^2 Saddle-Fin Transistor (SFT), 4F^2 Vertical Channel Transistor (VCT) is a preferred device to achieve a significant cell area reduction, lower bit line (BL) capacitance, and naturally immune to row hammer effect as well as short channel effect [1], as shown in **Fig. 2**. Hence, 4F^2 VCT DRAM is considered as one of the potential candidates for the next-generation 1T1C DRAM. Whereas, previous works [2-3] show that the inversion-mode (IM) VCT has limitations in the precise gate-to-channel alignment including a floating body effect (FBE) issue during a dynamic operation. On the contrary, junction-less (JL) VCT has a benefit in FBE suppression and achieving an easy gate-to-channel alignment, which is considered as a better choice for 4F^2 DRAM, as summarized in **Fig. 3**.

In this work, the high-performance VCT DRAM array consisting of orthogonal JL-GAA architecture combined with a hexagonal capacitor is demonstrated successfully. For the first time, we achieved an 8Gb full array JL-GAA VCT architecture with 9 orders of on-off ratio and ultra-low sub-threshold swing (*SS*) of 62.5 mV/dec. The influence of key process and device parameters have been discussed in detail. This work validated the outstanding performance of VCT aiming for the next generation of sub-10 nm DRAMs.

II. STRUCTURES

A. Full Array

3D full array structure of JL-GAA VCT and its corresponding x-sectional images are illustrated in **Fig. 4**. To fully utilize the cell efficiency, the high-*k* capacitor is designed as a hexagonal structure landing at VCT. A stack of node contact (NC) and landing pad should be inserted between the top Si pillar of VCT and the bottom electrode of the capacitor. It allows the checkerboard-type VCT array in conjunction with the hexagonal capacitors to realize 4F^2 DRAM architecture.

B. Vertical Channel Transistor

As can be seen in **Fig. 5**, we use an ALD TiN as word line (WL) gate material. Such a WL employs the GAA structure surrounding the gate dielectric over the Si pillar. WL-to-WL is fully isolated by the Si_xN_y material (**Fig. 5a**). BL is formed by controlling precise dose and depth profile of *N*+ hot implant at quad mode in **Fig. 5b**, which is also isolated to neighboring BLs with boron implant and shallow trench isolation (STI). The ratio of the WL to BL pitch size of the VCT cell was targeted to $\sqrt{3}:2$ for the integration requirement of combining orthogonal VCT and hexagonal capacitor. Thus, our Si pillar is more like a nanosheet (NS) structure instead of a nanowire (NW). It is also interesting to note that the final Si pillar shape looks like a dumbbell since the middle Si pillar is consumed during ALD+ISSG oxide formation at the channel region.

III. PROCESS DISCUSSION

A. Word-Line Isolation

To form the Si pillar array, the self-aligned double patterning (*x*-SADP) was implemented twice orthogonally. One of the most challenging processes is how to control the BL STI oxide (OX) etch profile precisely. In **Fig. 6**, when the OX etch profile is not vertical sufficiently (i.e., taper), thus a 'V'-shape oxide space profile would induce a serious WL-to-WL leakage due to less isolation margin. Such a problem can be resolved by tuning both ADI (After-development) and AEI (After-etch), as shown in **Fig. 7a**. It is confirmed electrically that a more vertical profile can minimize a parasitic WL-to-WL leakage current (from 200 μA to 2.5 pA), as illustrated in **Fig. 7b**.

B. Bit-Line Formation by N+ IMP

As described in **Fig. 2**, the BL formation of VCT is more difficult than that of conventional DRAMs due to the intrinsic buried structure. We have considered two different buried BL formation schemes: one is the metal BL scheme and the other is the *N*+ IMP BL scheme. Metal BL occupying a bowl shape trench helps to ensure a lower resistance but with a high risk of WL-to-BL leakage. *N*+ IMP BL has benefits in terms of process complexity and leakage minimization, however, a higher BL resistance (R_{BL}) is inevitable. To reduce the R_{BL} of *N*+ IMP BL, not only total implant dose and energy should be optimized but also hot implant with a quad mode is a mandatory option to avoid the ion damage and shadowing effect. R_{BL} with respect to different implant doses is also analyzed in **Fig. 8**. R_{BL} is reduced to 20% from the reference when the IMP dose is increased by 2x which leads to higher transistor drivability.

IV. Device Performance

A. Analysis of Key Device Parameters

The total leakage of access transistor is a crucial parameter for DRAM due to its influence on the retention time. A negative-boosted WL voltage is typically applied to reduce the total leakage by optimizing the sub-threshold, gate, junction leakages, and especially Gate Induced Drain Leakage (GIDL). Herein, two different GIDL mechanisms are described in **Fig. 9.** For conventional SFT devices, GIDL mainly comes from the transverse band-to-band tunneling (T-BTBT) in the gate/drain overlap region. On the other hand, for GAA VCT devices, GIDL mainly comes from the longitudinal band-to-band tunneling (L-BTBT) in the body/drain overlap region due to the full depletion of the gate/drain overlap region and the stronger gate controllability to the body/drain region [4]. Furthermore, we compare the energy band diagrams along the longitudinal direction of IM-GAA and JL-GAA in **Fig. 10.** JL-GAA VCT has a lower body energy band than IM-GAA VCT by the adoption of *N*-type body, which helps JL-GAA VCT to reduce the longitudinal electrical field for a small GIDL. Since other leakage components are comparable, hence, JL-GAA VCT is considered as a better choice for the $4F^2$ DRAM structure.

We also investigated the total leakage mechanism based on key device parameters such as channel length, source/drain (S/D) extension lengths and pillar dimensions, etc. **Fig. 11** shows the relationship between the extension length and GIDL current. With the extension doping peak adjusted by lower implant energy/dose, GIDL current can be minimized due to the larger band tunneling width inducing a lower BTBT generation rate. Furthermore, as pillar dimension is reduced, as shown in **Fig. 12**, the band narrowing leads to a higher L-BTBT due to a higher longitudinal electrical field. Therefore, a suitable pillar dimension combined with optimal S/D extension is necessary to obtain a minimal GIDL at the full depletion of the JL-GAA channel region.

B. Electrical Characteristics

After further optimizing the process and device conditions, a healthy *N*-type JL-GAA VCT is demonstrated with excellent electrical characteristics, as illustrated in **Fig. 13**. I_D-V_G plots are obtained by applying the NC=0.05/0.5/1V, BL=0V while sweeping WL voltage from -1V to 3V. Thanks to the GAA architecture, such a device could present an ultra-low *SS* value as low as 62.5 mV/dec, resulting in a high on-off ratio of 9 orders. To the best of our knowledge [5-8], the on-off ratio and *SS* values of our fabricated VCT rank as the 2nd best among the published Si-based vertical FETs, as compared in **Fig. 14**. Nevertheless, our JL-GAA VCT shows a relatively small on-state current (I_{on}) as shown in **Fig. 13**. We believed that the channel and S/D doping optimization with a contact resistance reduction via the laser annealing may boost the drivability further. Gate dielectric breakdown voltage (BV) is also measured and shown larger than 9V in **Fig. 15**. This result confirmed that our JL-GAA VCTs show outstanding device characteristics with reliable and robust process windows.

The hexagonal capacitor is also successfully demonstrated on the top of the orthogonal VCT structure with the NC and landing pad. The storage capacitance (C_s) is big enough and good uniformity within the wafer (WiW), which meets the DRAM electrical target requirements as illustrated in **Fig. 16**. Also, overall system level comparison between conventional $6F^2$ DRAM (SFT) and $4F^2$ VCT (JL-GAA) is summarized in **Fig. 17**. In comparison to conventional DRAM, JL-GAA VCT has advantages in gate controllability and RC delay points of view. Besides, the parasitic BL capacitance of VCT is also quite less than that of conventional one, which helps a bit-cell to obtain a higher BL sensing margin. Although the total WL capacitance of VCT is relatively high due to multiple parasitic components, actual WL coupling noise is not problematic because it can be compensated by neighboring WLs during the dynamic DRAM operation. In addition, $4F^2$ VCT shows a clear benefit over $6F^2$ DRAM in terms of tRCD, tCAS, tRP, and power consumptions according to overall system-level SPICE and PEX simulations.

IV. Conclusion

We have successfully fabricated the JL-GAA VCT cell array with a hexagonal capacitor for the next-generation $4F^2$ DRAM. Based on the discussion of key process and device parameters, we have achieved that our JL-GAA VCT obtains the breakthrough of 9 orders on-off ratio and 62.5 mV/dec *SS* which rank as the 2nd best among the state-of-the-art Si-based vertical GAA FETs. This work will be an important milestone of JL-GAA FETs for future sub-10 nm DRAM applications.

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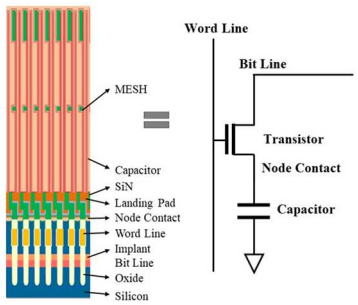


Fig. 1. 1T1C structure of DRAM. The word line connects to the gate of transistors, and the bit line/node contact connects to the source/drain of transistors.

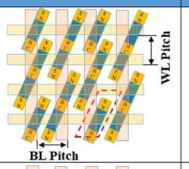
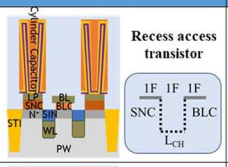
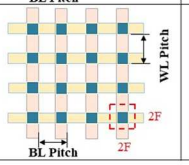
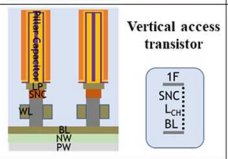
ITEMS	Layout	Profile map	Comments
$6F^2$ DRAM			Pros: ✓ Matured technology ✓ No floating body effect Cons: ✓ Lower bit-cell density ✓ Row hammer effect ✓ Short channel effect ✓ Process more complicated
$4F^2$ DRAM			Pros: ✓ Easier AA & NC patterns ✓ No BLC patterning ✓ higher bit density Cons: ✓ Difficult BL process ✓ Floating body effect

Fig. 2. Comparison between $6F^2$ DRAM and $4F^2$ DRAM.

Item	IM VCT	JL VCT
Working mode	Inversion mode	Accumulation mode
Conduction channel	Surface conduction	Bulk conduction
Mobility	Limited by surface scattering	Limited by impurity
Doping profile controlling	Difficult	Easy
Floating body effect	High	Low
SCE and Hot electron effect	Worse	Better
Leakage current	High	Extremely low
Fabrication challenge	High	Low

Fig. 3. Comparison between inversion-mode and junction-less VCT.

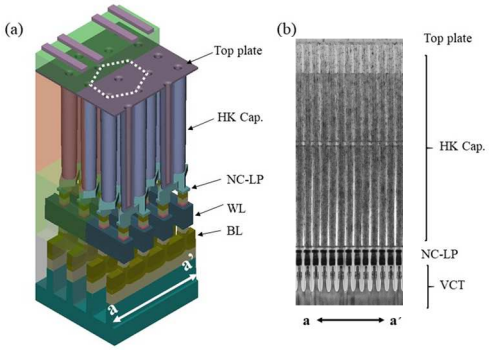


Fig. 4. (a) Full array of $4F^2$ VCT structure; (b) TEM of the VCT and capacitor structures.

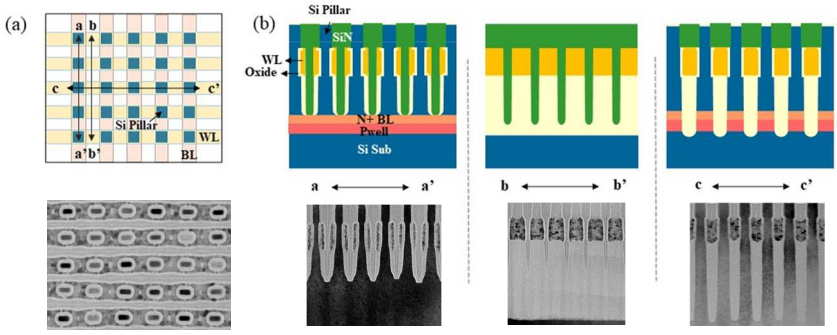


Fig. 5. (a) Layout and top-view image of $4F^2$ DRAM, (b) TEM cross-sections along a/b/c cut-lines.

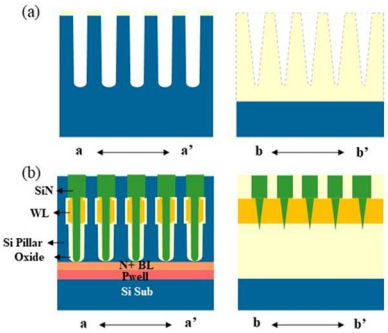


Fig. 6. Cartoon diagram of (a) bad BL STI profile and (b) final WL formation.

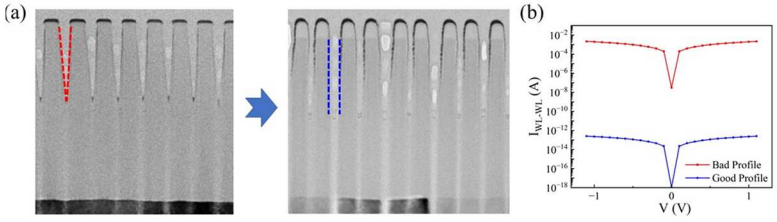


Fig. 7. (a) Process tuning of OX etch profile; (b) WL-WL LKG based on two OX etch profiles.

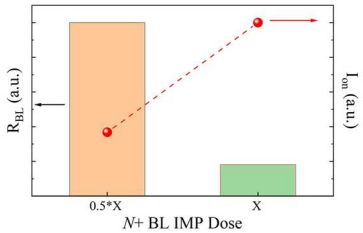


Fig. 8. BL resistance and on-state current in different BL IMP doses.

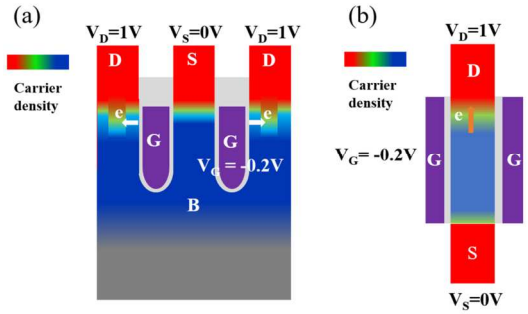


Fig. 9. Schematic diagram (a) GIDL of SFT induced by T-BTBT and (b) GIDL of VCT induced by L-BTBT.

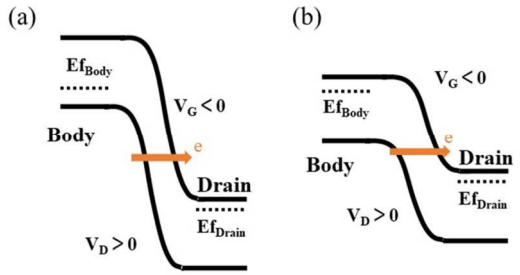


Fig. 10. Longitudinal energy band diagrams of (a) inversion-mode GAA VCT and (b) junction-less GAA VCT.

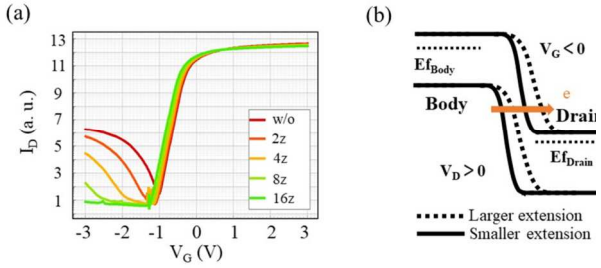


Fig. 11. Influence of source/drain extension on JL-GAA VCT: (a) device performance, z is the unit of S/D extension length; (b) longitudinal energy band diagrams.

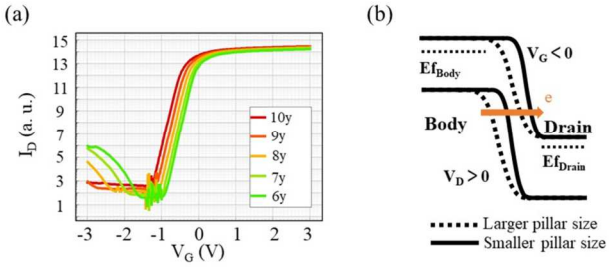


Fig. 12. Influence of pillar size on JL-GAA VCT: (a) device performance, y is the unit of pillar size; (b) longitudinal energy band diagrams.

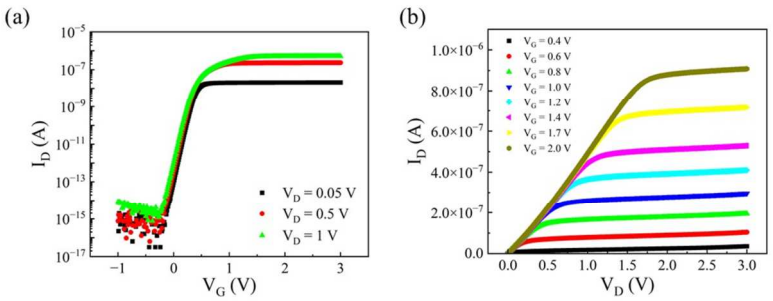


Fig. 13. (a) Transfer characteristics of JL-GAA VC; (b) Output characteristics of JL-GAA VCT.

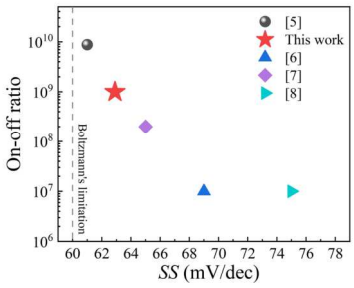


Fig. 14. Comparison of *SS* and on-off ratio in the published vertical channel transistors with this work.

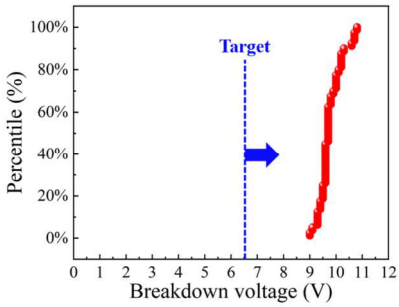


Fig. 15. Cumulative distribution function of breakdown voltage.

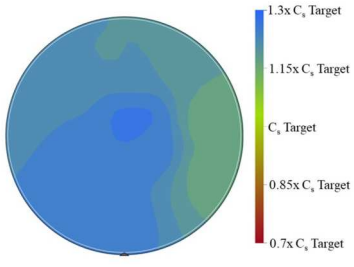


Fig. 16. Full map C_s distribution of the hexagonal capacitor.

Item	6F² Saddle Fin DRAM	4F² VCT DRAM
Gate controllability	Good	Excellent
Bit Cell RC	Worst due to tight design rule	Better with simple structure
WL Coupling	Row hammer risk	WL to WL coupling risk
Sense Margin	Lower sense Margin	Higher sense Margin due to lower BL coupling
Power Consumption	Worst	Better
tRCD	100%	96%
tCAS	100%	96%
tRP	100%	82%
tWR	100%	102%

Fig. 17. System-level comparison between $6F^2$ and $4F^2$ DRAM based on Si device data and circuit simulation.