

A 2.2 μ m 2-Layer Stacked HDR Voltage Domain Global Shutter CMOS Image Sensor with Dual Conversion Gain and 1.2e- FPN

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Abstract— The world's smallest HDR voltage-domain global shutter (VDGS) image sensor with 2.2 μ m pixel pitch was fabricated based on a 2-layer stacking process with Cu-to-Cu wafer bonding process. The pixel contains four storage capacitors within a 2.2 μ m pitch and has 1 $\times$ 2 shared structure to enable reducing transistor count in the second pixel layer. This design features single exposure dual conversion gain (DCG) capture, dual exposure capture and low noise performance, i.e. 1.2e-rms of pixel level fixed pattern noise (FPN) and 3.8e-rms of temporal noise.

I. INTRODUCTION

As technology advances, there are increasing interests of global shutter image sensors in applications such as machine vision, virtual and augmented reality, and autonomous driving, which require image capture capability without motion distortion and high shutter efficiency (SE). Moreover, these applications generally demand high level of system miniaturization that in turn pushes for continuous pixel pitch scaling, performance improvement and power/bandwidth optimization [1]. In general, global shutter image sensors can be categorized into charge domain global shutter (CDGS) sensors [2] and voltage domain global shutter (VDGS) sensors [3-8]. Similar to a CCD device, CDGS sensors use pinned storage nodes to store the photo-generated charges from the photodiodes (PDs). Although it can offer superior temporal noise and FPN similar to a rolling shutter sensor [2], pixel scalability and SE performance of CDGS sensors limit its adoption in the aforementioned applications [3]. Therefore, researchers have turned their attention to VDGS technology, which has inherently superior SE performance and also demonstrated great pixel scaling potentials thanks to modern wafer stacking and high density MIM (HD-MIM) technologies [3-4]. Unlike CDGS sensors, VDGS sensors convert charge signals into voltage signals and store them onto analog capacitors. Governed by the law of physics, this process introduces kTC noise and degrades the sensors' temporal noise performance. Moreover, the sample-and-hold (SH) transistors' mismatch also induces high level of FPN which will further limit the sensors' low light performance [3]. In this paper, a sensor with 2.2 μ m pixel pitch and four storage capacitors will be introduced to achieve the single capture DCG capability and an improved FPN performance of 1.2e-.

II. PIXEL STRUCTURE AND OPERATIONS

A. Circuit Schematic and Stacked Structure

As depicted in Fig.1, the sensor wafer includes a photodiode (PD), a transfer gate transistor (TG), a floating diffusion (FD), a reset transistor (RST), a dual conversion gain transistor (DCG), a 1st stage Source Follower (SF1), and a global shutter switch transistor (GS). The two vertically adjacent sensor wafer pixels' output nodes will be connected together to form a 1 $\times$ 2 shared design. On the ASIC wafer, within a 1 $\times$ 2 layout pitch, a bias transistor (Bias), four pairs of switch transistors (SHR, SHS), four pairs of storage capacitors (C_R , C_S), one 2nd stage source follower (SF2), one row select transistor (RS) and one clamping transistor (CLP) are included. One single stacked pixel level connection (SPLC) is used to connect every 1 $\times$ 2 shared sensor wafer pixel to the ASIC wafer side. Similar to that in [3], the same stacked structure (Fig.2) was used to obtain similar sensor performances (i.e. FWC, SE, NIR QE and MTF). In order to achieve single exposure DCG capability, four storage capacitors within a 2.2 μ m pitch are a must. Consequently, along with the ASIC wafer pixel structure change, the total number of transistors on the ASIC wafer within the pixel pitch is increased comparing to [3]. The 1 $\times$ 2 shared pixel design was chosen to mitigate this issue while guaranteeing no serious design rule violation. A higher density HDMIM process is adopted to further mitigate the severe storage capacitance loss when the number of capacitors within a pixel pitch increases from 2 to 4. However, even with the mitigation the unit capacitance was reduced to about 80% of that in [3]. As a result, a higher kTC induced temporal noise is observed, as will be discussed in Section III.

B. Timing Diagram and Operations

Since the pixel structure is 1 $\times$ 2 shared, there are in fact a pair of even and odd signals for each of the following controls: RST, DCG, TX and GS. The notation <0> is for the even signals and <1> for the odd signals, e.g. GS<0> and GS<1>. In one ASIC wafer pixel, there are four pairs of SHR and SHS signals and the numbers <0-3> are used to differentiate. In the timing generator design, these eight signals are interchangeable and can be regrouped as needed. Fig.3 illustrates a conventional global transfer timing of the proposed structure. As opposed to a no-share DCG VDGS

design [4], even and odd RST/DCG/TX signals toggle concurrently to ensure the correct global shutter operations. GS<0> and GS<1> are toggled sequentially to allow voltage sampling through the same SPLC and a total of eight samples will be sampled onto the corresponding storage capacitors, accounting for the even/odd PDs, the single exposure DCG operations and the correlated double sampling (CDS).

C. FPN Reduction

In some image sensor applications, the systems are more sensitive to FPN than the temporal noise. In turn, this requires continuous research effort on FPN reduction. Additionally, reduced unit capacitance leads to higher FPN number, which is also against the industrial trend. As briefly analyzed in Section I, the main FPN contribution in [3] is the mismatch between the SHR and SHS sampling switches and their charge injection, which is prevalent among a lot of similar pixel structures [3-5,7]. As given in the new pixel structure that has described in the paper, a new timing can be proposed to reduce the pixel's FPN. Fig. 4 depicts a simplified timing containing the controls of EN transistor and one set of SHR and SHS transistors. Instead of staying high across the whole global transfer timing, the EN signal toggles during the signal sampling operations and its falling edges leads the corresponding SHR and SHS falling edges, which results in a change of the sampling switch. The signal sampling is now accomplished by the only EN switch in the design instead of the two mismatched SHR and SHS switches. To the first order of approximation, the sampling procedure for CDS operation is free of mismatched charge injection and will yield lower FPN number.

III. MEASUREMENT RESULTS

This BSI VDGS is fabricated with 45nm sensor technology and a 65nm ASIC technology. The dynamic range, the signal-to-noise ratio plot, the temporal noise and FPN along with other pixel performances are measured and discussed below. The QE, MTF and Shutter efficiency are measured with 940nm light source.

A. Global shutter functionality and SE

Fig. 5 compares the global shutter operation and SE between a 2.2 μ m BSI VDGS [3] and a 1x2 shared 2.2 μ m BSI VDGS (this work). For both sensors, the dark region between blades appears completely black, indicating equally good SE performance. Moreover, no obvious even and odd pattern is observed in Fig.5(b), demonstrating a good overall global shutter functionality.

B. DR and SNR

Fig. 6 shows the sensor's measured SNR plots of the single exposure DCG capture and the dual exposure capture. The measurements show a single exposure capture DR of 69dB with an SNR knee point of 26dB at room temperature and a dual exposure capture DR of 85dB with an SNR knee point of 24dB at room temperature.

C. FPN reduction

Fig.7 compares the FPN performance between the timings of Fig.3 and Fig.4. The zoom-in view in the second image clearly shows improved FPN level, which is also confirmed by the FPN measurement results in Fig.8. These results have demonstrated the new timing's effectiveness in reducing the image FPN level.

D. Other pixel performances

Table I and Table II summarize this work and compare it with other recent publications in the area of global shutters. The QE, SE, MTF, FWC and PRNU performances are in line with its previous generation [3]. The temporal noise is measured as 3.8e- and the dark FPN is measured as 1.2e-, both at room temperature. The temporal noise is larger than [3] due to the increased kTC noise whereas the FPN performance is slightly smaller despite of smaller storage capacitor. This work has managed to achieve single exposure DCG capture with a smaller 2.2 μ m pixel pitch than [4].

IV. SUMMARY

To the knowledge of the authors, this work is the first to demonstrate a 2.2 μ m pitch, HDR VDGS sensor with low noise. This opens the door for the integration of other HDR technologies such as lateral overflow integrating capacitors (LOFIC), which will provide even higher DR to meet the requirements of future applications.

ACKNOWLEDGMENT

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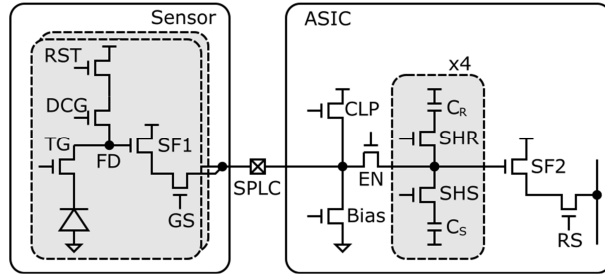


Fig. 1. Circuit schematic of the proposed voltage domain global shutter pixel.

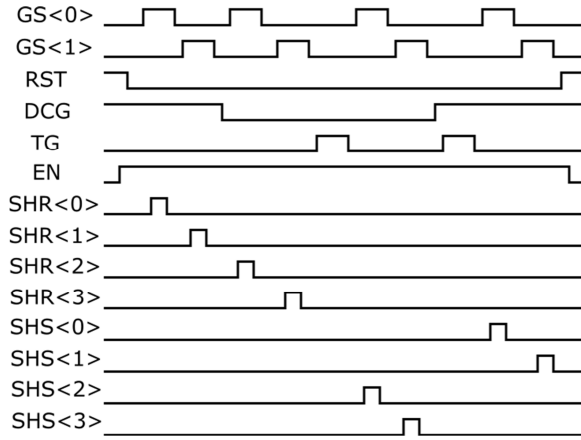


Fig. 3. Conventional timing diagram of 1x2 shared pixel global readout.

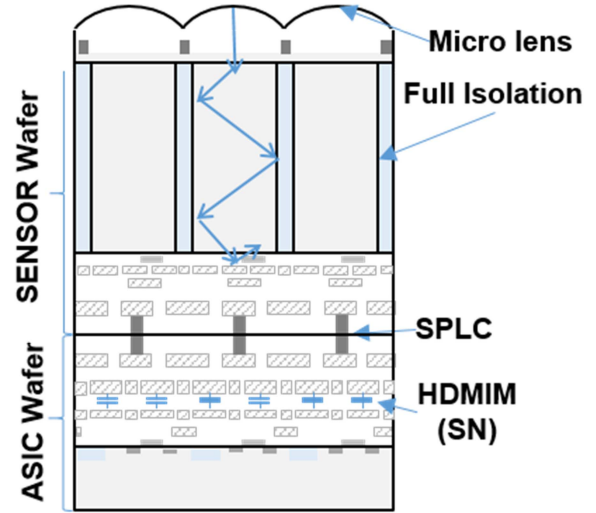


Fig. 2. Schematic cross section of stacked structure illustrating the sensor pixel and SN arrays.

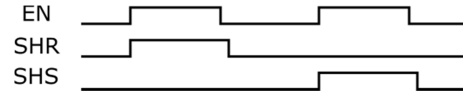


Fig. 4. FPN reduction technique.

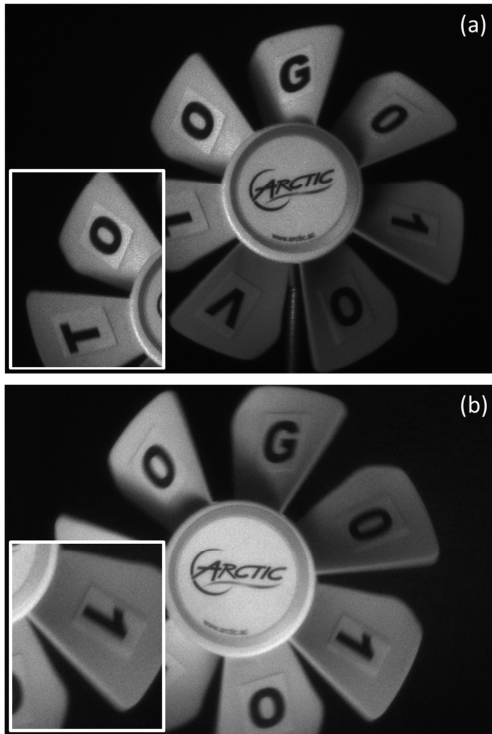


Fig. 5. Spinning fan images at 940nm wave length, F2.0, (a) previous work [3] (b) this work.

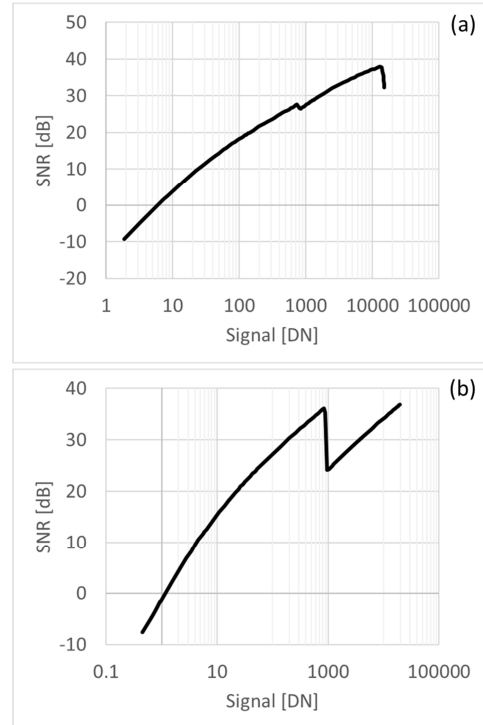


Fig. 6. SNR plots, (a) single exposure DCG mode (b) dual exposure mode.

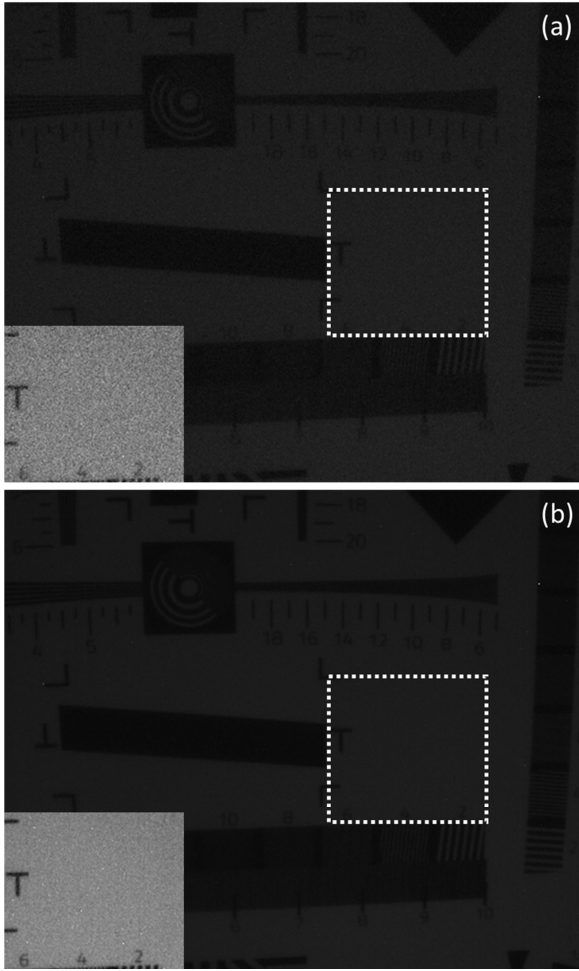


Fig. 7. Resolution chart at 940nm wave length, integration time=115 μ s, F2.0, 100 frame averaged, (a) the conventional timing, (b) the proposed timing.

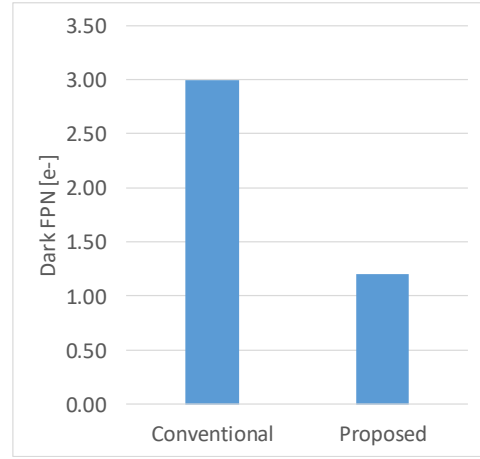


Fig. 8. FPN comparison

Parameter	Value
Pixel array pitch	2.2 μ m $\times$ 2.2 μ m
GS Mode	V-domain
Process Technology	TSMC 45n CIS/65n logic stacked BSI
Color Filter	Monochrome
CG	Dual CG : 60/200 μ V/e-
FWC	3500 e-/11000 e-
Effective Shutter efficiency @940nm	>100dB
RN	3.8 e-
FPN	1.2 e-
DC	25 e-/s @ 60°C
PRNU@940nm	0.6%
QE @940nm	38%
QE @850nm	53%
MTF@940nm, Ny/2	60% on Axis, 57%@30°

Table 1. Pixel performance summary.

	This work	IISW 2023 [4]	IEDM 2019 [3]	IEDM 2022 [5]	ISSCC 2019 [6]	ISSCC 2020 [7]	IISW 2019 [8]
Pixel pitch	2.2 μ m	3.45 μ m	2.2 μ m	1.8 μ m	2.7 μ m	2.3 μ m	4.0 μ m
C-mode / V-mode	V-mode	V-mode	V-mode	V-mode	V-mode	V-mode	V-mode
Resolution	1280x400	5M	1280x1024	1280x1024	1080x1280	1280x800	-
Number of storage Capacitors per pitch	4	4	2	2	2	2	4
Frame Rate	60fps	60 fps	120 fps	120 fps	120 fps	120 fps	-
FWC	11k e- @ LCG	20k e- @ LCG	12k e- @ LCG	14k e- @ LCG	10k e-	12k e- @ LCG	40k e- @ LCG
Effective Shutter efficiency @940nm	>100dB	>100dB	>100dB	130dB	86dB	85dB	140dB
RN	3.8 e- @ HCG	2.7 e- @ DCG	3.1 e- @ HCG	1.8 e- @ HCG	3.5 e-	2.1 e- @ HCG	5 e- @ HCG
FPN	1.2 e- @ HCG	1.4 e- @ DCG	1.7 e-	-	-	-	4.2 e- @ HCG
QE @940nm	38%	41%	38%	-	36%	42%	-
DR	85dB	90dB	71.74dB	77.8dB	110dB	75dB	102dB
SNR Tran	24dB	26dB	-	-	-	-	-

Table 2. Comparison of CIS performance.