Complementary Field-Effect Transistor (CFET) Demonstration at 48nm Gate Pitch for Future Logic Technology Scaling

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***Abstract*—** This study establishes the groundwork for an industry-applicable, integrated nanosheet-based monolithic CFET process architecture with a gate pitch of 48nm. By introducing the middle dielectric isolation, inner spacer, and n/p source-drain isolation, the vertically stacked nFET-on-pFET nanosheet transistors yield a survival rate of over 90% and demonstrate high on-state current with low leakage, achieving a healthy six-order of magnitude on/off current ratio. This work sets the stage for further CFET development and paves the way for a practical process architecture that can fuel future logic technology scaling and PPAC advancement.

I. INTRODUCTION

The architecture of transistors has evolved from planar to FinFET about a decade ago [1-2]. This transition was driven by the exceptional electrostatic integrity and scalability of FinFET devices, which enable continuous gate pitch and cell height scaling. As a result, FinFET architecture has been widely adopted in advanced technology nodes [3-5] to facilitate aggressive transistor scaling. Following a decade of fruitful utilization of multi-generation FinFET technology, the industry is getting ready to transition to a novel architecture for nanosheet field-effect transistors (NSFET) - commonly referred to as gate-all-around (GAA) [6-8]. The motivation behind this change is the expected superior gate controllability and device performance per unit area of NSFET, which is believed to surpass that of FinFET technology.

Beyond nanosheet CMOS technology, the complementary field-effect transistor (CFET) design presents a prospective solution for extending Moore's Law and caters to the increasing demand for improved performance and reduced power consumption in a compact form factor. Despite the anticipated rise in process complexity and cost associated with CFET fabrication, the vertically stacked nFET and pFET configuration illustrated in Figure 1 has generated significant interest as a promising device architecture [8-14]. This is owing to the noteworthy advantage of roughly 1.5 to 2 times higher density compared to the conventional CMOS architecture at the same gate pitch with n/p FET placed side by side. The reason for the density scaling benefit being limited to less than twice that of traditional CMOS with identical ground design rules is attributed to the amount of space needed for the vertical local interconnects that connect the upper nFET and lower pFET in the CFET setup, as depicted in Figure 2.

Earlier CFET device studies have shown that functional vertically stacked n/p transistors and inverters can be built on 300mm wafers with wider gate pitches [11-12]. However, the demonstration of CFET inverters and n/p transistors on the same wafer with gate pitches around 50nm, which is pertinent to industry-level advanced node scaling, has not been accomplished due to the challenges associated with integrating vertical local connection and isolation between stacked nFET and pFET [13-14].

In this work, we address a specific set of challenges for integrating nanosheet-based monolithic CFET (mCFET) with a gate pitch of 48nm. Our primary aim is to present industry-relevant CFET transistors that employ vertical stacking of n/p source-drain (SD) epitaxy with dielectric isolation between them, which achieves a remarkable six-order of magnitude on/off current ratio and low leakage. To accomplish this, we introduce the middle dielectric isolation (MDI), inner spacer (INSP), and n/p SD isolation (SD-ISO) in our nanosheet channel mCFET structure. Survival rates exceeding 90% have been achieved for nFET and pFET, providing a robust foundation for future mCFET advancement, which involves challenges of integrating other essential architectural features to unleash the potential of CFET and fully realize its PPAC capabilities.

II. DEVICE FABRICATION

Figure 3 shows the simplified mCFET process flow for fabricating the nanosheet-based monolithic 3-D stacked nFET-on-pFET devices reported in this study. Figure 4(a) depicts a comparison between NSFET and mCFET by showcasing the initial SiGe/Si superlattice stacks that will undergo down-stream processes to become nanosheet channels. The SiGe/Si superlattice stack for mCFET includes a high Ge% SiGe layer as a placeholder for MDI formation after SD etch. Figure 4(b) compares an in-house lattice mismatch index between the traditional NSFET stack and the mCFET stack, showing comparable crystalline quality of SiGe/Si superlattice stacks between two configurations. After laying the nanosheet superlattice stack, a state-of-the-art process from advanced technology nodes is employed to define the critical dimension for building CFET transistors with 48nm gate pitch and 15nm gate length, which includes nanosheet stack patterning by EUV lithography, shallow trench isolation (STI) formation, dummy gate patterning by EUV lithography, low-k dielectric gate spacer deposition, and SD etching for subsequent SD epitaxy (EPI) growth.

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To establish foundation for low leakage CFET transistors, a unique process for forming middle dielectric isolation (MDI) and inner spacer (INSP) has been developed, which leverages the selectivity of SiGe etching to the Ge%. In vertically patterned SD formation, a sidewall liner is first employed to cover the top nanosheet during PMOS SiGe:B epitaxy (pEPI) growth on the bottom nanosheet. Then, A controlled dielectric etching process is utilized to create the n/p SD isolation (SD-ISO) layer before NMOS Si:P epitaxy (nEPI) growth. The ability to control the depth of the dielectric recess is essential to achieving high-quality nEPI and ensuring optimal nFET performance while minimizing variability. Following the SD formation, device wafers in this work undergoes a conventional advanced CMOS process that includes several stages such as ILD0 planarization, removal of dummy gates, release of Si nanosheet channel, formation of interlayer (IL) and high-k dielectrics, V_T tunning, deposition of work function metal (WFM) and metal gate (MG), creation of SD contact, and integration of middle-of-line (MOL) and back-end-of-line (BEOL) interconnect.

Figure 5 shows the inline cross-section TEM images illustrating key mCFET process features described above. To obtain early electrical validation for the health of our mCFET transistors, nFET and pFET device wafers are processed separately with simplified V_T tunning schemes to set desired V_T and adjusted metallization drain (MD) etch to form proper SD contact. In Figure 6(a), an nFET is shown schematically with a single nMG and a vertically stacked nEPI-ISO-pEPI that has a shallow MD to create a contact connection to nEPI. On the other hand, Figure 6(b) shows a pFET with a pMG and a deep MD to aid in the contact connection to pEPI. In Figure 7, an integrated nFET-on-pFET is depicted with patterned n/p V_T and a dual MD landing solution to exhibit both nFET and pFET on the same wafer for subsequent development.

III. Electrical Characteristics

This study showcases the electrical properties of nFET and pFET created through mCFET process, as explained in the device fabrication section above. Figure 8 displays the survival rate of vertically stacked nFET-on-pFET Si nanosheet transistors, which have been evaluated based on their physical electrical parameters and fundamental transistor functionality. The detailed survival criterion is also presented in Figure 8. It is observed that both nFET and pFET have exhibited a survival rate of over 90%, indicating a robust process at this initial developmental stage.

To illustrate the intrinsic transistor I_d-V_g and I_d-V_d characteristics, the 75th percentile performance dies from nFET and pFET wafers are selected. Figure 9 displays the I_d-V_g characteristics of the vertically stacked nFET-on-pFET Si nanosheet transistors with a 48nm gate pitch and L_g ~ 15nm. The gate-all-around nanosheet architecture provides excellent electrostatics resulting in subthreshold swings (SS_{sat}) of 75mV/dec and 73mV/dec for nFET and pFET, respectively. Also, the drain-induced barrier lowering (DIBL) for nFET and pFET are 50mV/V and 45mV/V, respectively. Figure 10 depicts the I_d-V_d characteristics from the same selected nFET and pFET, demonstrating high on-state performance. Given that the hole mobility μ_h is lower than the electron mobility μ_e on the (100) plane, and with the majority of conduction in our nanosheet channel occurring on the (100) plane rather than the (110) plane, it is expected that the intrinsic performance of nFET will be better than that of pFET. However, we observe pFET performance is slightly better than nFET. To investigate this discrepancy, we extract the gate-bias dependent channel resistance R_{ch} and gate-bias independent parasitic resistance R_p to understand the resistance partition. R_p is calculated as the y-intercept from a linear resistance (V_{ds} = 50 mV) plotted against $1/V_{od}$ (where V_{od} is the gate overdrive voltage). Figure 11 depicts the R_p of the nFET and pFET. This graph clearly illustrates a degraded nFET parasitic resistance, which can be improved by optimizing the n/p SD ISO dielectric recess profile and nEPI deposition.

Figures 12 to Figure 15 display the I_{on}-I_{off} and V_T-I_{off} curves for both nFET and pFET. To expand the range of I_{on}-I_{off} and V_T-I_{off}, a gate offset voltage (V_{Goff}) ranging from 0 to ±0.15V is employed on top of the 0.75V V_{dd}. A multi-V_T flow is under development to demonstrate nFET and pFET on the same wafer as illustrated in Figure 7. In addition, we compare the devices reported in this work to the previously reported mCFET with a scaled gate pitch [13-14] in Table 1. The results show that the devices in this study exhibit higher on-state current, similar SS_{sat} at shorter L_g, and well targeted V_T with balanced I_{on} and I_{off} between nFET and pFET.

IV. Conclusion

In this work, we set the basis for a practical monolithic CFET process architecture that can be utilized by industries. Our study produces vertically stacked nFET-on-pFET Si nanosheet transistors that exhibit high on-state current and low subthreshold leakage. These results open doors for future advancements in CFET technology by introducing additional essential architectural features to fully unlock its PPAC potential.

Acknowledgment

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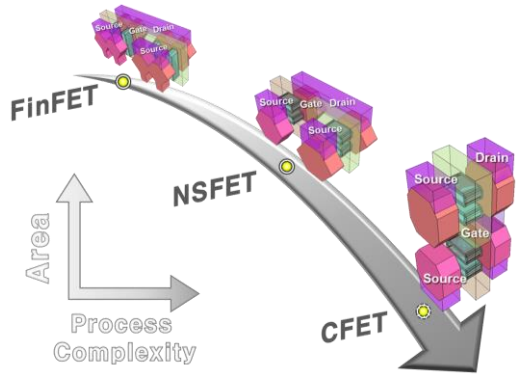


Fig. 1. Device architecture evolution from FinFET, Nanosheet FET (NSFET), to 3-D stacked CFET architecture. Novel transistor architecture innovations keep fueling the energy to drive relentless Moore' Law scaling.

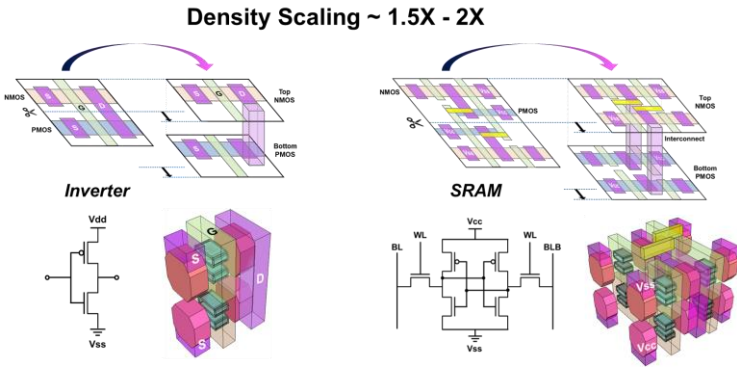


Fig. 2. By vertically stacking a nFET on top of a pFET with applicable vertical local interconnects, CFET has great potential to achieve approximately 1.5 to 2 times density scaling for standard cells and SRAM bitcells as compared to the conventional CMOS architecture.

- Substrate preparation
- SiGe/Si superlattice growth
- Nanosheet stack patterning
- STI formation
- Gate patterning
- Gate spacer deposition
- Source-drain (SD) etch
- Middle dielectric isolation
- Inner spacer formation
- N/P SD vertical patterning
- PMOS SD epitaxy growth
- N/P SD isolation formation
- NMOS SD epitaxy growth
- ILD0 planarization
- Si nanosheet channel release
- IL/High-k dielectric formation
- V_T tunning
- WFM and Metal gate deposition
- SD contact formation
- MOL & BEOL integration

Fig. 3. Monolithic 3-D stacked CFET process flows for top nFET and bottom pFET device fabrication.

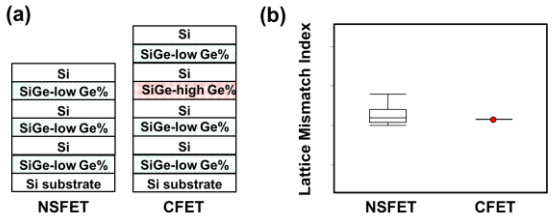


Fig. 4. (a) Illustration of the stacking scheme for conventional NSFET and CFET SiGe/Si superlattices. In contrast to the conventional 3-sheet nanosheet stacking, CFET utilizes a high Ge% layer to form MDI. (b) Comparison of the in-house lattice mismatch index between our NSFET and mCFET stack as a sanity check on crystalline quality of the SiGe/Si superlattice stacks.

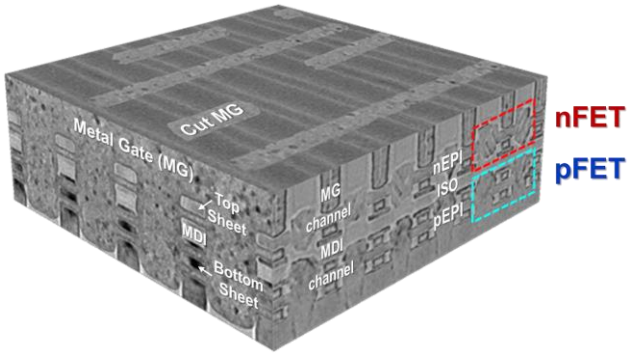


Fig. 5. TEM demonstration of monolithic CFET with a gate pitch of 48nm. The device architecture design includes nFETs placed above pFETs, and both types of transistors are surrounded by a single metal gate.

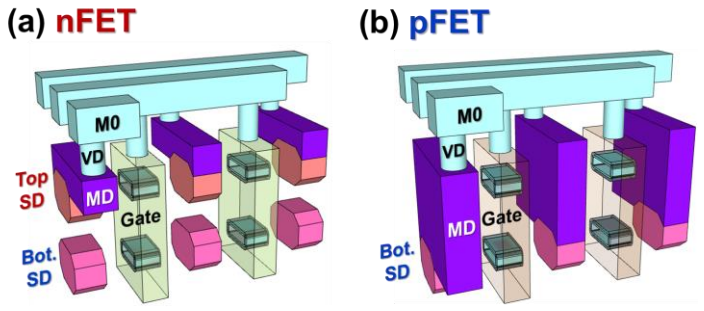


Fig. 6. Schematics of 3-D stacked CFET structure with (a) top nFET SD contacted and (b) bottom pFET SD contacted to conduct the electrical characterization for nFET and pFET, respectively.

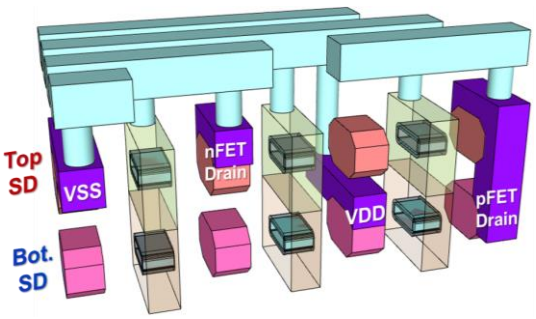
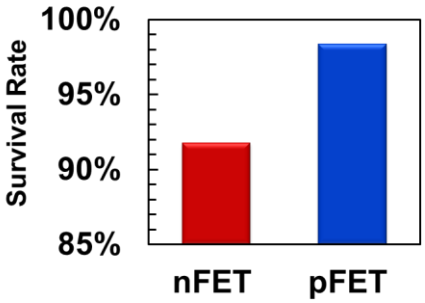


Fig. 7. Schematics of 3-D stacked CFET structure with both top nFET and bottom pFET SD contacted for device characterization on the same wafer.

Scaled CFET	This work	VLSI 2023 [14]	IEDM 2021 [13]
Organization	TSMC	IMEC	Intel
Device Architecture	Monolithic CFET	Monolithic CFET	Monolithic CFET
Top Device	1-Nanosheet Si nFET	1-Nanosheet Si nFET	2-Nanoribbon Si nFET
Bottom Device	1-Nanosheet Si pFET	1-Nanosheet Si pFET	2-Nanoribbon Si pFET
Gate Pitch	48 nm	48 nm	55 nm
Gate Length	15 nm	27 nm	19 nm
Inner Spacer	Yes	No	?
N/P SD Epitaxy Stacking	Yes	No	Yes
N/P SD Isolation	Yes	No	No
nFET SS	75 mV/dec	70 mV/dec	70 mV/dec
pFET SS	73 mV/dec	73 mV/dec	N/A
	@ V_{ds} = ± 0.75V	@ V_{ds} = ± 0.7V	@ V_{ds} = 0.65V
I_{OFF} (nFET): I_{OFF} (pFET)*	~ 1:1	~ 1:100 – 1:1000	N/A
nFET I_{ON}*	> 1 mA/μm	~ 0.4 mA/μm	~ 0.2 mA/μm
pFET I_{ON}*	> 1 mA/μm	~ 0.1 mA/μm	N/A
Note: V_{gs_off} as V_g @ I_{ds} = 1 nA/μm	@ V_{gs} – V_{gs_off} = V_{ds} = ± 0.75V	@ V_{gs} – V_{gs_off} = V_{ds} = ± 0.7V	@ V_{gs} – V_{gs_off} = V_{ds} = 0.65V

Table 1. Comparisons of the scaled mCFET transistors reported in this work to the previous studies. [Note: I_{ON}* and I_{OFF}* are read from the figure scale in cited literatures.]



Parameter	Survival criterion
$V_{T, lin}$ (V), $V_{T, sat}$ (V)	$\|V_{T, lin}$ (V)$\|$<1 and $\|V_{T, sat}$ (V)$\|$<1
DIBL (mV/V)	10< DIBL (mV/V) <200
Subthreshold Swing (SS_{sat})	10 <SS_{sat} <100
Rch (Ω*um)	10< Rch (Ω*um) <350

Fig. 8. Survival rate and survival criterion of the vertically stacked nFET-on-pFET Si nanosheet transistors.

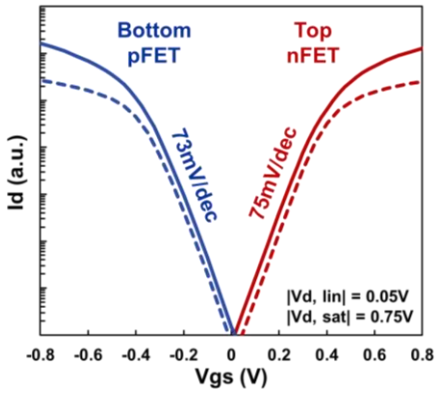


Fig. 9. I_d-V_{gs} characteristics of vertically stacked nFET-on-pFET Si nanosheet transistors with a gate pitch of 48nm & L_g~15nm from the 75-percentile performance die showing excellent sub-threshold swings.

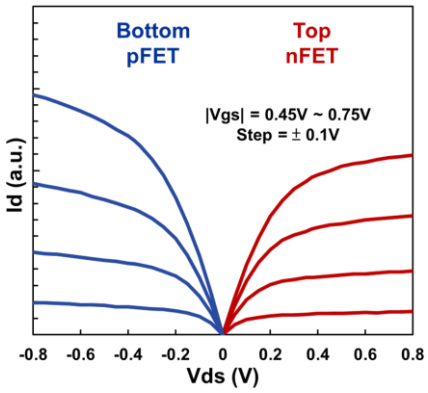


Fig. 10. I_d-V_{ds} characteristics of vertically stacked nFET-on-pFET Si nanosheet transistors with a gate pitch of 48nm & L_g~15nm from the 75-percentile performance die showing high on-state performance.

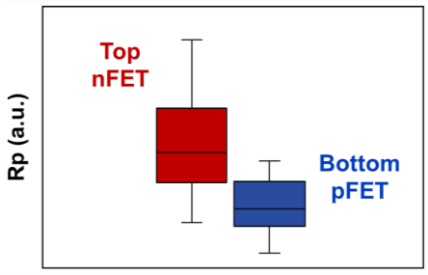


Fig. 11. Extracted parasitic resistance R_p showing degraded nFET R_p compared to pFET.

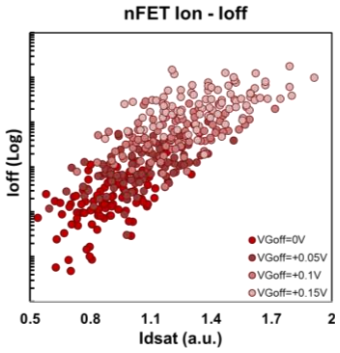


Fig. 12. Top nFET I_{on}-I_{off} curve from vertically stacked nFET-on-pFET Si nanosheet transistors.

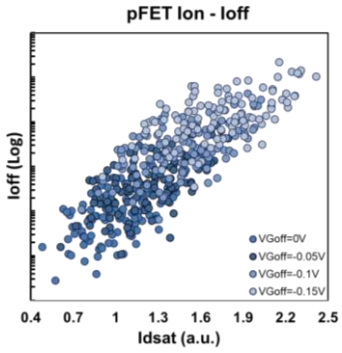


Fig. 13. Bottom pFET I_{on}-I_{off} curve from vertically stacked nFET-on-pFET Si nanosheet transistors.

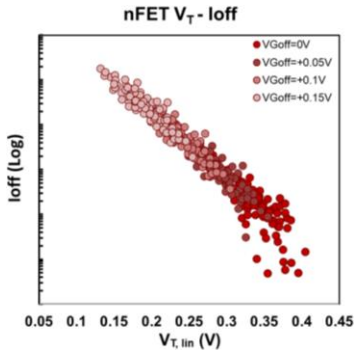


Fig. 14. Top nFET V_T-I_{off} curve from vertically stacked nFET-on-pFET Si nanosheet transistors.

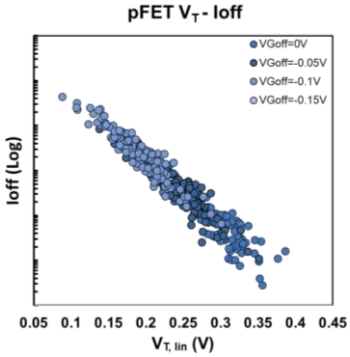


Fig. 15. Bottom pFET V_T-I_{off} curve from vertically stacked nFET-on-pFET Si nanosheet transistors.